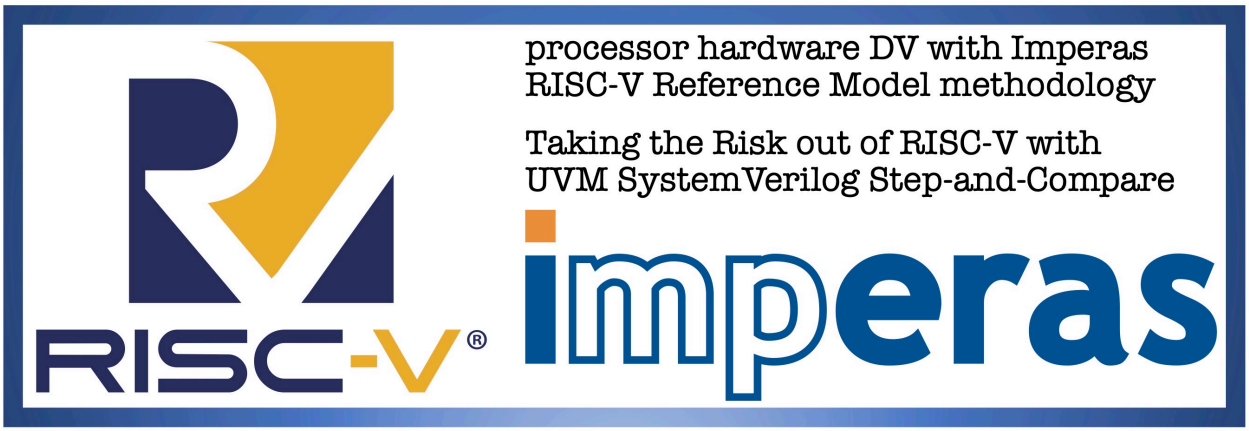

Imperas Leading RISC-V CPU Reference Model for Hardware Design Verification Selected by Mellanox

Verification tools and golden reference model provide support for RISC-V custom instruction extensions and full processor design verification

Oxford, United Kingdom, April 21st, 2020 — Imperas Software Ltd., the leader in virtual platforms and high-performance software simulation, today announced that Mellanox Technologies a leading supplier of high-performance, end-to-end smart interconnect solutions for datacenter servers and storage systems, has selected the Imperas advanced hardware verification of RISC-V processors. RISC-V as an open ISA (Instruction Set Architecture) permits many configuration and options for processor implementation and microarchitectural features, in addition to extension with custom instructions. Simulation based methodologies are the foundation for hardware design verification (DV) throughout the semiconductor industry in achieving first pass prototype success.

The Imperas RISC-V models are provided in source form, which allows users to adapt and extend for custom configurations independently. The model can be encapsulated in a UVM environment for a complete SystemVerilog DV flow. By using the RISC-V reference model in a side-by-side configuration with the target RTL, it is possible to run step-and-compare analysis either interactively or in automated regression tests for continuous integration. Typical processor verification plans include rigorous testing of the RTL with comparison to a golden reference model, using a range of stimulus inputs such as the RISC-V International Association Compliance suite, directed tests, and constrained random Instruction Stream Generator (ISG) tests, like the Google open-source project known as Google RISC-V DV-ISG see https://github.com/google/riscv-dv.

“We have selected Imperas simulation tools and RISC-V models for our design verification flow because of the quality of the models and the ease of use of the Imperas environment,” said **Shlomit Weiss, Senior Vice President of Silicon Engineering at Mellanox Technologies**. “Imperas reference model of the complete RISC-V specification, the ability to add our custom instructions to the model and their experience with processor RTL DV flows were also important to our decision.”

“Open ISAs like RISC-V need to pioneer compliance collectively as opposed to established ISAs, which are controlled by single companies that are motivated to ensure that all designs being shipped work correctly,” said **Dan Mandell, Senior Analyst of IoT & Embedded Technology at VDC Research**. “The RISC-V Compliance Suite, which is aimed at addressing this obstacle, is developing with contributions by organizations like Imperas Software providing new tools and solutions for verification and simulation reference models.”

"The Imperas RISC-V reference model covers the complete envelope of the standard ISA features and options, plus our software analysis tools help designers evaluate and profile custom extensions," said **Simon Davidmann, CEO at Imperas Software Ltd**. "We are proud to support the world class engineering team at Mellanox with the Imperas golden reference model for RISC-V."

About Imperas

Imperas is revolutionizing the development of embedded software and systems and is the leading provider of RISC-V processor models and virtual prototype solutions. Imperas, along with Open Virtual Platforms (OVP), promotes open source model availability for a spectrum of processors, IP vendors, CPU architectures, system IP and reference platform models of processors and systems ranging from simple single core bare metal platforms to full heterogeneous multi-core systems booting SMP Linux. All models are available from Imperas at www.imperas.com and the Open Virtual Platforms (OVP) website.

For more information about Imperas, please see www.imperas.com. Follow Imperas on LinkedIn, twitter @ImperasSoftware and YouTube.